

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant:	Cheng-Lien Chiang		
Assignee:	Bridge Semiconductor Corporation		
Title:	SEMICONDUCTOR PACKAGE DEVICE THAT INCLUDES AN INSULATIVE HOUSING WITH A PROTRUDING PERIPHERAL PORTION		
Serial No.:	Unknown	Filed:	Herewith
Examiner:	Unknown	Group Art Unit:	Unknown
Atty. Docket No.:	BDG005-1-4		

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COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**

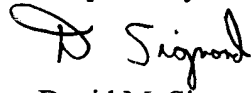
Pursuant to Applicant's duty of disclosure under 37 C.F.R. § 1.56 and §§ 1.97-1.98, Applicant hereby submits the enclosed Form PTO-1449.

Copies of documents cited on the enclosed Form PTO-1449 are not enclosed because they were previously cited by or submitted to the U.S. Patent Office in U.S. Application Serial No. 10/059,686 filed January 29, 2002 and/or U.S. Application Serial No. 10/042,812 filed January 9, 2002. The above-identified application is a continuation of the '686 application, which is a continuation of the '812 application.

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, an admission that any of these documents, alone or in any combination, is considered to be material to patentability, an admission that any of these documents is prior art as to the above-identified application, or an admission against interest in any manner.

This Information Disclosure Statement is filed before the mailing date of a first Office Action. Accordingly, no fee is due.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "D. Sigmond". The signature is written in a cursive, flowing style.

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Form PTO-1449 U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No. BDG005-1-4		Serial No.	
<b>INFORMATION DISCLOSURE STATEMENT</b> (Use several sheets if necessary)				Applicant Cheng-Lien Chiang			
				Filing Date		Group Art Unit	
<b>U.S. Patent Documents</b>							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,081,520	01/1992	Yoshii et al.	357	80	
	AB	5,241,133	08/1993	Mullen, III et al.	174	52.4	
	AC	5,394,303	02/28/95	Yamaji	361	749	
	AD	5,665,652	09/1997	Shimizu	438	127	
	AE	5,674,785	10/1997	Akram et al.	437	217	
	AF	5,744,827	04/28/98	Jeong et al.	257	686	
	AG	5,744,859	04/1998	Ouchida	257	668	
	AH	5,804,771	09/1998	McMahon et al.	174	255	
	AI	5,811,879	09/1998	Akram	257	723	
	AJ	5,949,655	09/1999	Glenn	361	783	
	AK	6,013,877	01/2000	Degani et al.	174	264	
	AL	6,143,588	11/2000	Glenn	438	116	
	AM	6,159,770	12/2000	Tetaka et al.	438	112	
	AN	6,274,927	08/2001	Glenn	257	680	
<b>Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)</b>							
	AO	Crowley, "Socket Developments for CSP and FBGA Packages," Chip Scale Review, May 1998, pp. 37-40.					
	AP	Forster, "Socket Challenges for Chip-Scale Packages," Chip Scale Review, May 1998, pp. 43-47.					
	AQ	Amagai, "Chip-Scale Packages for Center-Pad Memory Devices," Chip Scale Review, May 1998, pp. 68-77.					
	AR	Vandavelde et al., "The PSGA, a Lead-Free CSP for High Performance & High Reliable Packaging," Proceedings of the 2001 International Symposium on Microelectronics, October 9, 2001, pp. 260-265.					
Examiner			Date Considered				
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*Examiner Initial	Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)		
	AA	U.S. Application Serial No. 09/865,367, filed May 24, 2001, entitled "Semiconductor Chip Assembly With Simultaneously Electroplated Contact Terminal and Connection Joint"	
	AB	U.S. Application Serial No. 09/864,555, filed May 24, 2001, entitled "Semiconductor Chip Assembly with Simultaneously Electrolessly Plated Contact Terminal and Connection Joint"	
	AC	U.S. Application Serial No. 09/864,773, filed May 24, 2001, entitled "Semiconductor Chip Assembly With Ball Bond Connection Joint"	
	AD	U.S. Application Serial No. 09/878,649 filed June 11, 2001, entitled "Method of Making a Semiconductor Chip Assembly with a Conductive Trace Subtractively Formed Before and After Chip Attachment"	
	AE	U.S. Application Serial No. 09/878,626 filed June 11, 2001, entitled "Method of Connecting a Conductive Trace to a Semiconductor Chip"	
	AF	U.S. Application Serial No. 09/917,339 filed July 27, 2001, entitled "Method of Connecting a Bumped Compliant Conductive Trace to a Semiconductor Chip"	
	AG	U.S. Application Serial No. 09/927,216 filed August 10, 2001, entitled "Semiconductor Chip Assembly with Hardened Connection Joint"	
	AH	U.S. Application Serial No. 09/939,140 filed August 24, 2001, entitled "Semiconductor Chip Assembly with Interlocked Conductive Trace"	
	AI	U.S. Application Serial No. 09/962,754 filed September 24, 2001, entitled "Method of Connecting a Conductive Trace and an Insulative Base to a Semiconductor Chip"	
	AJ	U.S. Application Serial No. 09/972,796 filed October 6, 2001, entitled "Method of Connecting a Bumped Compliant Conductive Trace and an Insulative Base to a Semiconductor Chip"	
	AK	U.S. Application Serial No. 09/997,973 filed November 29, 2001, entitled "Method of Connecting a Bumped Conductive Trace to a Semiconductor Chip"	
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	5,149,958	09/1992	Hallenbeck et al.	250	216		
	AB	5,264,714	11/1993	Nakaya et al.	257	78		
	AC	5,405,809	04/1995	Nakamura et al.	437	209		
	AD	5,834,835	11/1998	Maekawa	257	680		
	AE	5,834,843	11/1998	Mori et al.	257	723		
	AF	5,859,471	01/1999	Kuraishi et al.	257	666		
	AG	5,893,723	04/1999	Yamanaka	438	65		
	AH	6,265,770	07/2001	Uchiyama	257	698		
	AI							
	AJ							
	AK							
	AL							
	AM							
<b>Foreign Patent Documents</b>								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AN	JP-57100761	06/1982	Japan	H01L	27/14		X
	AO							
<b>Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)</b>								
	AP							
	AQ							
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	3,627,901	12/1971	Happ	174	52 PE		
	AB	3,678,385	07/1972	Bruner	324	158 F		
	AC	3,930,114	12/1975	Hodge	174	52 FP		
	AD	4,506,238	03/1985	Endoh et al.	333	138		
	AE	5,157,480	10/1992	McShane et al.	357	74		
	AF	5,207,102	05/1993	Takahashi et al.	73	727		
	AG	5,436,500	07/1995	Park et al.	257	696		
	AH	5,677,566	10/1997	King et al.	257	666		
	AI	5,866,939	02/1999	Shin et al.	257	666		
	AJ	5,894,107	04/1999	Lee et al.	174	52.2		
	AK	5,951,804	09/1999	Kweon et al.	156	244.12		
	AL	6,114,770	09/2000	Akram et al.	257	784		
	AM	6,130,116	10/2000	Smith et al.	438	127		
	AN	6,232,152	05/2001	DiStefano et al.	438	124		
	AO	6,297,543	10/2001	Hong et al.	257	666		
	AP	6,303,997	10/2001	Lee	257	778		
	AQ	6,326,700	12/2001	Bai et al.	257	790		
	AR	6,445,077	09/2002	Choi et al.	257	786		
	AS	6,455,356	09/2002	Glenn et al.	438	123		
	AT	6,468,836	10/2002	DiStefano et al.	438	128		
<b>Foreign Patent Documents</b>								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AU	JP-01128897	05/1989	Japan	B42D	15/02		X
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	6,001,671	12/1999	Fjelstad	438	112		
	AB	6,025,650	02/2000	Tsuji et al.	257	786		
	AC	6,281,568	08/2001	Glenn et al.	257	684		
	AD							
	AE							
	AF							
	AG							
	AH							
	AI							
	AJ							
	AK							
	AL							
	AM							
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	AA	6,198,171	03/2001	Huang et al.	257	787		
	AB	6,218,728	04/2001	Kimura	257	693		
	AC							
	AD							
	AE							
	AF							
	AG							
	AH							
	AI							
	AJ							
	AK							
	AL							
	AM							
<b>Foreign Patent Documents</b>								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AN	JP-06097352	04/1994	Japan	H01L	23/50	X	
	AO							
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